



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR    | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|-------------------------|---------------------|------------------|
| 09/859,575      | 05/15/2001  | William J. Hamilton JR. | PD-00W071           | 4120             |

7590

07/18/2003

Raytheon Company  
Intellectual Property  
MC Eo/EI/EI50  
P.O. Box 902  
El Segundo, CA 90245

EXAMINER

YAM, STEPHEN K

ART UNIT

PAPER NUMBER

2878

DATE MAILED: 07/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/859,575

Applicant(s)

HAMILTON ET AL.

Examiner

Stephen Yam

Art Unit

2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 22 April 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

This action is in response to Amendments and remarks filed on April 22, 2003. Claims 1--23 are currently pending.

#### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki et al. Japanese Publication No. 06-037291.

Regarding Claims 1, 2, 6, and 7, Ozaki et al. teach (see Fig. 2c) a hybrid array structure comprising a circuit array (6, 6B, 6C) of an array of circuits, each of the circuits comprising a first support-structure interconnect location (a first bump (8)) and a second supported-structure interconnect location (a second bump (8) on the same island), a supported array (three islands) comprising an array of supported islands with each support island having at least one supported element therein and at least one detector element for each circuit, comprising a first region (3) (see Fig. 2b) and a second region (2), wherein the first regions and second regions of each island are discontinuous from each other, and a bump interconnect structure (5, 8) extending between each of the circuits and its respective supported element, comprising a first bump interconnect (8B) extending from the first supported-structure interconnect location to the first region of its

Art Unit: 2878

respective supported element, and a second bump interconnect ((8) adjacent to (8B) in Fig. 2c) extending from the second supported-structure interconnect location to the second region of its respective supported element. Ozaki et al. also teach the circuit array (6, 6B, 6C) as a signal processing circuit (see Paragraph 0001) embedded in a silicon substrate (7) (see Paragraph 0018). Regarding Claim 2, Ozaki et al. teach the first region (3) comprising a first semiconductor region (see Paragraph 0020- "n type") and the second region (2) comprising a second semiconductor region (see Paragraph 0020- "p type"). Regarding Claim 6, Ozaki et al. teach the hybrid microelectronic array structure as planar (see Fig. 1). Regarding Claim 7, Ozaki et al. teach the hybrid microelectronic array structure as curved (see Fig. 1 and 3a,b). Ozaki et al. do not teach the processing circuitry formed using microelectronic integrated circuitry. It is well known in the art to use microelectronic integrated circuits for fulfilling processing requirements, due to the common use, lower cost, and ease of fabrication of microelectronic integrated circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a microelectronic integrated circuit for each signal processing element in the structure of Ozaki et al., to provide a low-cost signal-processing solution using common and well-known design and fabrication techniques.

Regarding Claim 3, Ozaki et al. teach the structure as taught in Claim 1, according to the appropriate paragraph above. Ozaki et al. do not teach the circuit comprising an electrical interface circuit and an input/output element supported on the electrical interface circuit. It is well known in the art that optical detectors and signal processing circuits require an electrical power source in order to function and an input/output element to output the detected/processed signal. It would have been obvious to one of ordinary skill in the art at the time the invention

Art Unit: 2878

was made to provide an electrical interface circuit and an input/output element in the structure of Ozaki et al., to provide both electrical power to operate the structure components and a signal output characteristic of the detection and processing functions performed by the structure, basic well-known elements of a detector array.

3. Claims 4 and 8-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki et al. in view of Watton et al. US Patent No. 6,388,256.

Regarding Claim 4, Ozaki et al. teach the structure in Claim 3, according to the appropriate paragraph above. Ozaki et al. do not teach the processing circuitry formed using readout integrated circuitry. Watton et al. teach (see Fig. 1) a structure with a readout integrated circuit array (11) and a detector array comprising an array of detector islands (5, 8) having at least one detector element (2) therein, and a bump interconnect structure (13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a readout integrated circuit array for signal processing and retrieval as taught by Watton et al. in the structure of Ozaki et al., to process the output detector signals (see Col. 3, lines 4-5) and provide a high-performance, integrated, detector array.

Regarding Claims 8-10 and 12-15, Ozaki et al. teach (see Fig. 2c) a hybrid array structure comprising a circuit array (6, 6B, 6C) of an array of circuits, each of the circuits comprising a first detector interconnect location (a first bump (8)) and a second detector interconnect location (a second bump (8) on the same island), a detector array (three islands) comprising an array of detector islands with each detector island having at least one detector element therein and at least

Art Unit: 2878

one detector element for each circuit, comprising a first semiconductor region (3) (see Fig. 2b) and a second semiconductor region (2), wherein the first semiconductor regions and second semiconductor regions of each island are discontinuous from each other, and a bump interconnect structure (5, 8) extending between each of the circuits and its respective detector element, comprising a first bump interconnect (8B) extending from the first detector interconnect location to the first semiconductor region of its respective detector element, and a second bump interconnect ((8) adjacent to (8B) in Fig. 2c) extending from the second detector interconnect location to the second semiconductor region of its respective detector element. Ozaki et al. also teach the circuit array (6, 6B, 6C) as a signal processing circuit (see Paragraph 0001) embedded in a silicon substrate (7) (see Paragraph 0018). Regarding Claim 9, Ozaki et al. teach the first semiconductor region as an n-doped semiconductor (see Paragraph 0020- "n type") and the second semiconductor region as a p-type semiconductor (see Paragraph 0020- "p type"). Regarding Claim 10, Ozaki et al. teach (see Fig. 2c) an electrically nonconducting support material (7) lying between the circuit array (6) and the detector array (1, 2, 3, 4, 5, 9). Regarding Claim 12, Ozaki et al. teach the readout integrated circuit array and the detector array each substantially planar (see Fig. 1). Regarding Claim 13, Ozaki et al. teach (see Fig. 3a and 3b) the circuit array being curved (see different-length bumps (8)), and the detector array (1, 2, 3, 4, 5, 9) being curved. Regarding Claim 14, Ozaki et al. teach the first and second bump interconnect each comprising Indium (see Paragraph 0002, 0017, 0018). Regarding Claim 15, Ozaki et al. teach the detector array type consisting of mercury-cadmium-telluride (see Paragraph 0016 and 0020). Ozaki et al. do not teach the processing circuitry formed using readout integrated circuitry. Watton et al. teach (see Fig. 1) a structure with a readout integrated circuit array (11)

Art Unit: 2878

and a detector array comprising an array of detector islands (5, 8) having at least one detector element (2) therein, and a bump interconnect structure (13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a readout integrated circuit array for signal processing and retrieval as taught by Watton et al. in the structure of Ozaki et al., to process the output detector signals (see Col. 3, lines 4-5) and provide a high-performance, integrated, detector array.

Regarding Claims 16 and 17, Ozaki et al. teach (see Fig. 2c) a hybrid array structure comprising a circuit array (6, 6B, 6C) of an array of circuits, each of the circuits comprising a first detector interconnect location (a first bump (8)) and a second detector interconnect location (a second bump (8) on the same island), a detector array (three islands) comprising an array of detector islands with each detector island having at least one detector element therein and at least one detector element for each circuit, comprising a first semiconductor region (3) (see Fig. 2b) and a second semiconductor region (2) wherein each detector island is electrically isolated from each of the other detector islands except through the circuit array, and an interconnect structure (5, 8) extending between each of the circuits and its respective detector element, comprising a first interconnect (8B) extending from the first detector interconnect location to the first semiconductor region of its respective detector element, and a second interconnect ((8) adjacent to (8B)) extending from the second detector interconnect location to the second semiconductor region of its respective detector element. Ozaki et al. also teach the circuit array (6, 6B, 6C) as a signal processing circuit (see Paragraph 0001) embedded in a silicon substrate (7) (see Paragraph 0018). Regarding Claim 17, Ozaki et al. teach the first and second interconnect of each interconnect structure are each electrically conducting bump interconnects (see Paragraph 0002).

Art Unit: 2878

Ozaki et al. do not teach the processing circuitry formed using readout integrated circuitry.

Watton et al. teach (see Fig. 1) a structure with a readout integrated circuit array (11) and a detector array comprising an array of detector islands (5, 8) having at least one detector element (2) therein, and a bump interconnect structure (13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a readout integrated circuit array for signal processing and retrieval as taught by Watton et al. in the structure of Ozaki et al., to process the output detector signals (see Col. 3, lines 4-5) and provide a high-performance, integrated, detector array.

Regarding Claims 18-22, Ozaki et al. teach providing a circuit array (6, 6B, 6C) of an array of circuits, each of the circuits comprising a first detector interconnect location (a first bump (8)) and a second detector interconnect location (a second bump (8) on the same island), preparing (see Fig. 2a) a detector array (three islands) comprising an array of detector islands with each detector island having at least one detector element therein and a detector element for each circuit, comprising a first semiconductor region (2) (see Fig. 2b) and a second semiconductor region (3) wherein each detector island is electrically isolated from each of the other detector islands except through the circuit array, depositing the first semiconductor region onto a detector substrate (1, 9) (see Paragraph 0016), depositing the second semiconductor region onto the first semiconductor region (see Paragraph 0016), defining detector islands as electrically isolated segments (see Fig. 2b) including a segment of the first semiconductor region overlying the detector substrate and the second semiconductor region overlying the first semiconductor region (see Fig. 2b), forming on each detector element a first interconnect ((5)-left) to the first semiconductor region and a second interconnect ((5)-2<sup>nd</sup> from left) to the second



Art Unit: 2878

semiconductor region, and joining the detector array to the readout integrated circuit array by an interconnect structure to form the structure, by joining each first interconnect to the respective first detector interconnect region and joining each second interconnect to the respective second detector interconnect location (see Fig. 3a and 3b). Ozaki et al. also teach the circuit array (6, 6B, 6C) as a signal processing circuit (see Paragraph 0001) embedded in a silicon substrate (7) (see Paragraph 0018). Regarding Claim 19, Ozaki et al. teach the first and second interconnect of each interconnect structure are each electrically conducting bump interconnects (see Paragraph 0002). Regarding Claim 20, Ozaki et al. teach the step of defining detector islands including the step of forming a trench (cut) through the first and second semiconductor region and into the detector substrate (see Paragraph 0012 and 0021). Regarding Claim 21, Ozaki et al. teach removing the detector substrate after preparing the detector array (see Fig. 3a → Fig. 3b). Regarding Claim 22, Ozaki et al. teach deforming the structure into a curved geometry (see Fig. 3a and 3b). Ozaki et al. do not teach the processing circuitry formed using readout integrated circuitry. Watton et al. teach (see Fig. 1) a structure with a readout integrated circuit array (11) and a detector array comprising an array of detector islands (5, 8) having at least one detector element (2) therein, and a bump interconnect structure (13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a readout integrated circuit array for signal processing and retrieval as taught by Watton et al. in the structure of Ozaki et al., to process the output detector signals (see Col. 3, lines 4-5) and provide a high-performance, integrated, detector array.

Regarding Claims 11 and 23, Ozaki et al. in view of Watton et al. teach the structure and method in Claims 8 and 18, according to the appropriate paragraph above. Ozaki et al. and

Art Unit: 2878

Watton et al. do not teach an electrical conductor interconnecting all the first detector interconnect locations. It is well known in the art that a detector array contains addressing and bussing components to direct the outputs of specific detector elements using common multiplexing and decoding techniques, where all the array elements are electrically interconnected through a multiplexer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to interconnect all the first detector interconnect locations in the structure and method of Ozaki et al. in view of Watton et al., to minimize the output lines necessary to output detector information and simultaneously providing access to specific detector elements.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki et al. in view of Shieh et al. US Patent No. 5,621,225.

Ozaki et al. teach the structure as taught in Claim 3, according to the appropriate paragraph above. Ozaki et al. do not teach the electrical interface circuit as a driver integrated circuit and the input/output element as an emitter. Shieh et al. teach (see Fig. 6) a structure with an array of driver integrated circuits (26), a supported array (14) of emitters (see Col. 4, lines 25-29), and a bump interconnect structure (32) (see Fig. 4). It would have been obvious to one of ordinary skill in the art at the time the invention was utilize emitters and driver integrated circuits as taught by Shieh et al. for the structure of Ozaki et al., to provide a reliable LCD display device while maintaining a compact package size and cost effectiveness (see Shieh et al.- Col. 3, lines 43-46).

***Response to Arguments***

5. Applicant's arguments filed April 22, 2003 have been fully considered but they are not persuasive.

Regarding Applicant's arguments on the Ozaki reference, Applicant argues that it is improper to utilize both Fig. 2 and Fig. 4 together in the rejection, as they are incompatible. Examiner asserts that the inventive feature of Ozaki is to split the structure into three distinct sections, and that the interconnect method between the invention and the prior art, which Examiner utilized Fig. 4 for in the prior Office Action, is identical. However, in response to Applicant's confusion, Examiner has revised the rejection to use the elements in Fig. 2 to point out the invention, using the same elements as indicated in Fig. 4. As none of the associated elements have changed between Fig. 2 and Fig. 4, Examiner deems that the subject matter within the rejection is equivalent to the prior Office Action, therefore the rejection is made final.

Applicant also argues that Ozaki does not teach "the first bump interconnect extending *to the first region*". Examiner asserts that since the first region and the second region are in contact with each other, as seen in Fig. 2b, the first bump interconnect does indeed extend to the first region, as it contacts the photodetector (4). In addition, Examiner affirms that "extending to" does not imply that the first bump interconnect is in electrical contact with the first region, but rather simply reaches the area of the first region.

Applicant also requests that Examiner presents a reference for the teachings that are deemed "well known" prior art in the rejection of Claim 1. Examiner refers Applicant to Bryan et al. US Patent No. 6,458,547, who teaches a microelectronic integrated circuit array (see Col.

Art Unit: 2878

38, lines 35-41 and 60-63) of processing elements (see Col. 38, lines 22-23) attached to an array of photodiode cells (104) (see Fig. 1 and 2), who also teaches using microelectronic integrated circuitry to provide low costs (see Col. 38, lines 60-61) and to use a fabrication process which is well known and practiced in the art (see Col. 39, lines 3-6). Hence, Examiner submits that using microelectronic integrated circuitry is well known in the art for cost and fabrication advantages.

Regarding Applicant's arguments on the Watton reference, Applicant argues that the structure of Watton does not indicate a "physically discontinuous" structure or an "array of detector islands" from the reference numbers (5,8) and suggests that Fig. 4-5 demonstrate that (5,8) do not create isolated islands. Examiner asserts that the array of detectors are indeed islands as they are isolated from each other using the interconnect channel which contains a dielectric material (10) (see Fig. 1) which isolates each of the adjacent islands (see Col. 5, lines 33-37). Hence, the array of detector islands are also physically discontinuous as they are separated by the channel (8), especially with its layer of isolating dielectric material (10). Even in Fig. 4 and 5, it is seen that the detectors form an array or "island" of individual detectors.

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392,

Art Unit: 2878

170 USPQ 209 (CCPA 1971). Since both references refer to an array of detector islands, they are within similar arts and are permissible for combination.

Applicant also requests that Examiner presents a reference for the teachings that are deemed "well known" prior art in the rejection of Claims 11 and 23. Examiner refers Applicant to Battersby US Patent No. 5,742,044, who teaches (see Fig. 1) a detector array (array of (10)) contains addressing (22, 23, 25, 26) and bussing (24, 28, 35, 36) components to direct the outputs of specific detector elements using common multiplexing and decoding techniques, where all the array elements are electrically interconnected through a multiplexer (22, 23), with an electrical conductor (12) interconnecting all the first detector interconnect locations (cathode of (11)). Hence, Examiner submits that using an electrical conductor interconnecting all the first detector interconnect locations is well known in the art for switching purposes for readout of a detector array.

Regarding Applicant's arguments on the Shieh reference, Applicant argues that Shieh does not teach the limitations of the claim language. Examiner submits that Ozaki teaches the claim limitations except for what is provided by Shieh, as explained above in the rejection of Claims 1 and 5.

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2878


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (703)308-4852. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

SY  
July 2, 2003



**DAVID PORTA**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**